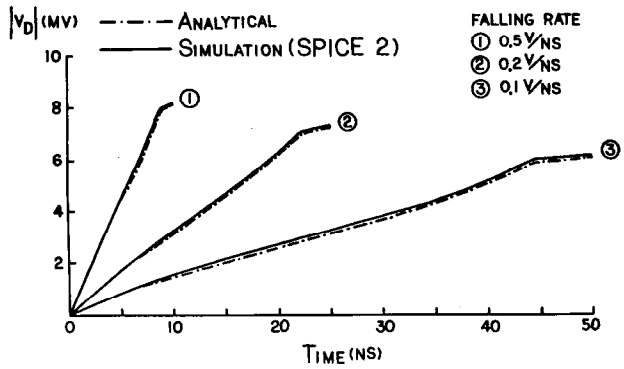


Fig. 3. Comparison of the analytic and computer simulated transient responses for three different gate voltage falling rates. The parameters for Figs. 3 and 4 are $V_S = 0$, $C_L = 2$ pF, $V_{T0} = 0.60$ v, $W = 4$ μm, $L = 3.3$ μm, $L_D = 0.35$ μm, and $\beta = 30.3$ μA·V$^{-2}$.

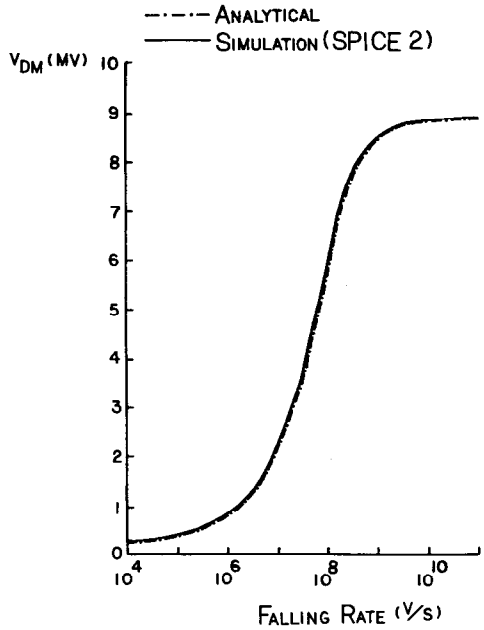


Fig. 4. Comparison of the analytic and computer simulated results of the error voltage as a function of the gate voltage falling rate.

## III. Comparison with Computer Simulation

To validate the model, compute simulations using the SPICE 2G [6], [7] circuit-simulation program have been performed. The circuit configuration for computer simulations is the same as that of Fig. 1.

The analytical transient response, (6), and computer simulated results for three different gate voltage falling rates 0.1 V/ns, 0.2 V/ns, and 0.5 V/ns are shown in Fig. 3. The close agreement between the analytical analysis and the computer simulation is evident. Another comparison is shown in Fig. 4. The error voltage is plotted against the gate voltage falling rate for both the analytical and simulation results. Fig. 5 shows the measured data and calculated result from the analytical model (8). Good agreement is found.

## IV. Conclusion

An analytical expression for the switch-induced error voltage on a switched capacitor is presented. Computer simulation and experiment justify the validity of the analysis. The compact

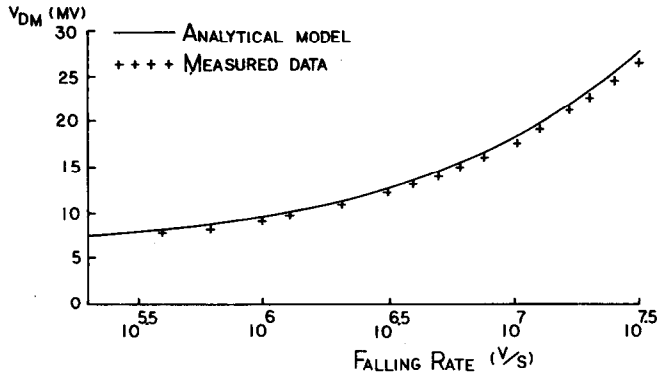


Fig. 5. Measured and calculated error voltages as functions of gate voltage falling rate. The parameters are $V_S = 0$, $C_L = 24.5$ pF, effective $C_{ol} = 195$ fF (including parasitic probe capacitance), $V_{TO} = 0.70$ V, $W = 40$ μm, $L = 5.1$ μm, $L_D = 0.45$ μm, $t_{ox} = 85$ nm, and $\beta = 295$ μA·V$^{-2}$.

expression (8) should be convenient in the analysis of switched-capacitor circuits, such as A/D, D/A converters, and filters.

## Acknowledgment

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# Transition to Chaos in a Simple Nonlinear Circuit Driven by a Sinusoidal Voltage Source

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***Abstract*—A circuit composed of a sinusoidal voltage source, a linear resistor, a linear inductor, and a diode in series is investigated. Subharmonic solutions of various orders have been found by computer simulations and there is evidence for the presence of chaotic solutions. The diode model used involves a nonlinear capacitor. The transition to chaos follows the same pattern as for iterated maps on an interval.**

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## I. Introduction

In [1], [2], laboratory measurements on the circuit of Fig. 1 have been reported which indicate the presence of chaotic solutions. This came as a surprise, because the educated electronics engineer expects a periodic steady state with the same period $T = 2\pi/\omega$ as the voltage source. Such a "normal" behavior turns out to be present as long as the source amplitude $V_0$ is sufficiently small. When $V_0$ reaches a certain value $E_1$, the period of the steady state doubles and thus for $V_0$ just above $E_1$ the steady state is a 1/2 subharmonic. Such a phenomenon is called a bifurcation. When $V_0$ is further increased, a whole sequence $E_k$ of period-doubling bifurcations has been observed, leading to 1/4-, 1/8-, 1/16-, $\cdots$ subharmonics. The $E_k$ appear to converge to a value $E_\infty$. Above $E_\infty$ no steady state is observed anymore, the solutions are chaotic, except for some small intervals, called windows, where period doubling occurs again, but starting from a 1/3-subharmonic, or a 1/5-subharmonic, etc.

The diode used in [1], [2] was a varactor, which has a large nonlinear reverse-bias junction capacitance. It has been pointed out in [3] that a common junction diode causes the same phenomena and that the crucial effect is the transit time of the junction. In any case, it is clear that without some parasitic effect of the diode there would neither be subharmonic nor chaotic solutions [4].

The experimentally observed qualitative behaviour of the solutions show a close resemblance with the behaviour of point sequences generated by iterated noninvertible maps on an interval of the real line, for which a rigorous mathematical theory exists [5]. By modeling the transit time of the diode by a sharp delay, the two phenomena have been related in [6].

From a circuit-theoretic point of view, a sharp delay is not satisfactory. Rather, the transit time should be modelled by a nonlinear capacitor. The purpose of this letter is to give evidence that such a model is capable of reproducing the same phenomena. This evidence is produced by computer simulations.

## II. Computer Simulations

We have computed time-domain solutions of the circuit of Fig. 1 by SPICE2. SPICE uses the model of Fig. 2 for the diode, where the nonlinear resistor has the constitutive relation

$$i_1 = I_s \cdot (\exp(u/nV_T) - 1) \tag{1}$$

the nonlinear capacitor that models the reverse bias junction capacitance is defined by

$$q_2 = C_{j0} \cdot \Phi \left(1 - (1 - u/\Phi)^{1-m}\right)/(1-m) \qquad \text{for } u < \Phi$$
$$q_2 = C_{j0} \cdot \Phi/(1-m) \qquad \text{for } u > \Phi \tag{2}$$

and the nonlinear capacitor that models the transit time by

$$q_3 = \tau I_s \ (\exp(u/nV_T) - 1). \tag{3}$$

We have chosen the following values for the parameters:

$$I_s = 8.3 \times 10^{-15}\ \text{A}, \quad r_s = 9.6\ \Omega, \quad n = 1, \quad \tau = 4 \times 10^{-6}\ \text{s},$$
$$C_{j0} = 300\ \text{pF}, \quad m = 0.4, \quad \Phi = 0.75\ \text{V}.$$

They model a varactor diode.

We have computed $i(t)$ for a large number of different source amplitudes $V_0$. The results are reported in Fig. 3. Above each value of $V_0$ on the horizontal axis, the 30 values $i(n*T)$ for $n = 1000, 1001, \cdots, 1029$ are reported. We start with $n = 1000$ rather than $n = 1$ in order to leave sufficient time for the solution to reach its steady state, if there is any. If the steady state is periodic with period $T$, then the 30 points $i(n*T)$ are identical. This is the case for $V_0 < 0.84$ V in Fig. 3. If the steady state is

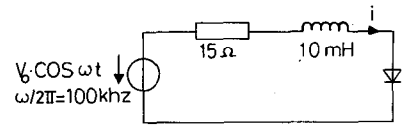


Fig. 1. Series circuit with diode.

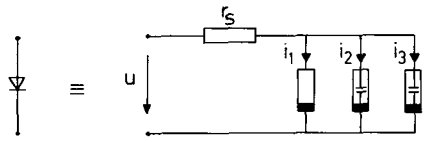


Fig. 2. SPICE model for the diode.

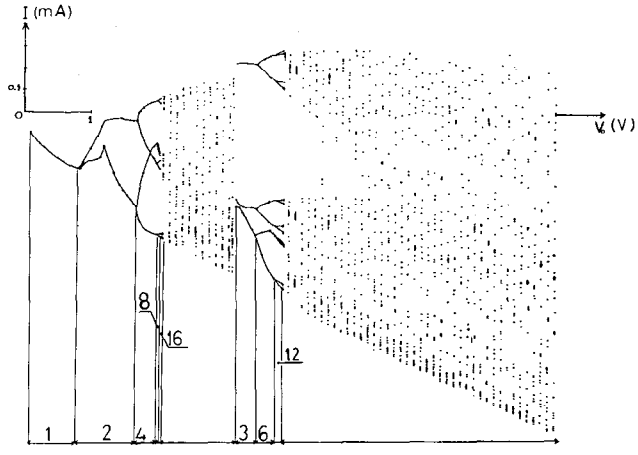


Fig. 3. Bifurcation diagram for the current.

periodic with period $2*T$, then two sets of 15 identical points $i(n*T)$ are obtained, which is the case for $0.84\ \text{V} < V_0 < 1.71\ \text{V}$. Hence at $V_0 = 0.84$ V the graph of Fig. 3 bifurcates.

The period doubling bifurcations are clearly visible in Fig. 3 up to the 1/16-subharmonic. Later on, all points $i(n*T)$ are distinct. This means that either the steady state has not yet been reached or the steady state has a period longer then $29*T$, or there is no periodic steady state at all. The similarity with the bifurcation diagrams of [5] suggests the presence of chaotic solutions. A window with 1/3-, 1/6-, 1/12-, $\cdots$ subharmonics is visible within the chaos.

## III. Conclusion

We have found by computer simulation a period-doubling route to chaos, as well as windows within the chaos, for the circuit of Fig. 1.

The diode model involves a nonlinear capacitor rather than a sharp delay.

## Acknowledgment

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