`Physlock`: An Entry–Level Low-Cost Lock-In Amplifier

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The design of a simple, entry level low–cost, stand–alone lock-in amplifier is described. The instrument is useful for detecting and amplifying signals that are frequency synchronized with a reference signal. It is particularly important for detecting and measuring small signals in the presence of large noise. The design is based on a modulator/demodulator integrated circuit and uses a minimum number of components to accomplish input amplification, phase-sensitive detection, low-pass filtering, and dc amplification of the output signal. `Physlock` is based on the chip `AD630` and will be helpful in teaching students about low–level signal detection which is commonplace in numerous tasks in the experimental physics laboratory. It can also be used in the research laboratory (see specs below).

Major specifications of `PhysLock`

Power	220 V, 50 Hz
Reference signal amplitude	> 1 V
Dynamic Range	60 dB to 70 dB
DC gains	$1\times$ or $10\times$
AC input gains	$1\times$, $10\times$, $50\times$, $100\times$, $200\times$ $500\times$, $1000\times$, $2000\times$, $5000\times$, $10000\times$
Low pass filter time constants	1 s, 470 ms, 47 ms, 10 ms, 4.7 ms, 1 ms, 470 μs, 100 μs, 50 μs,10 μs
Form of input signal	Low frequency (< 1 KHz) periodic signal (square to sine converter is also provided).

1 Theory of Operation

Figure 1 shows the block diagram of the lock–in amplifier. The important components of this circuit will now be described. Each component is shown inside a dashed box for greater clarity.

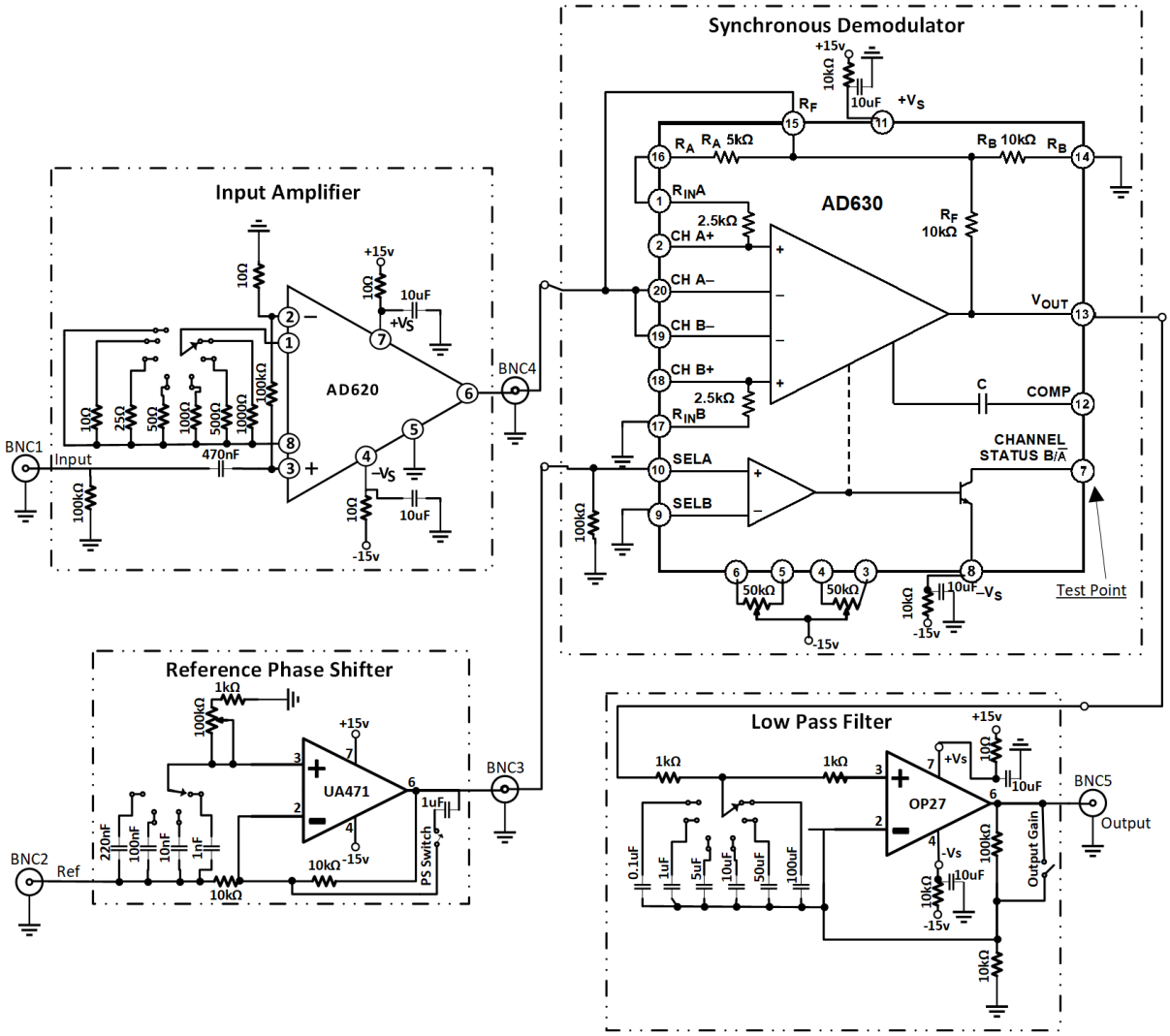

Figure 1: Block diagram of the lock-in amplifier. The input signal is first amplified and then demodulated with a reference signal of known frequency. The output of this stage is then passed through a low pass filter which returns the final DC output. The input and output gains, phase shift of the input signal and the low pass filter threshold can be varied using controls provided on the instrument.

1.1 Input Amplifier

The raw input signal is applied on the `BNC1` connector and passes through an amplifier circuit. It's gain can be easily changed to 1×, 10×, 50×, 100×, 200× 500×, 1000×, 2000×, 5000×, or 10000× by changing the feedback resistance of the amplifier chip `AD620`.

1.2 Reference Phase Shifter

The reference signal applied on the BNC2 connector passes through a buffered phase-shifter. The phase-shifter can also be bypassed by using the PS Switch. This circuit has unity gain.

1.3 Synchronous Demodulator

The functional block diagram of the AD630 chip (see Figure 2) shows the pin connections for the demodulation process. The individual A and B channel preamps, the switch, and the integrator output amplifier are combined in to a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

The basic function of the AD630 may be easier to recognize as two gain amplifiers, which can be inserted into a signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic demodulation function.

Figure 2(a) shows a test configuration to understand the basic functionality of AD630. The comparator selects one of the two input stages to complete an operational feedback connection around AD630. Likewise, when Channel B is selected, the R_A and R_F resistors are connected for inverting feedback as shown in the inverting gain diagram in Figure 2(a). When the sign of comparator input is reversed, Input B is deselected and Input A is selected. The new equivalent circuit is the noninverting gain configuration shown in Figure 2(c). (See AD630's data sheet [1] for further details).

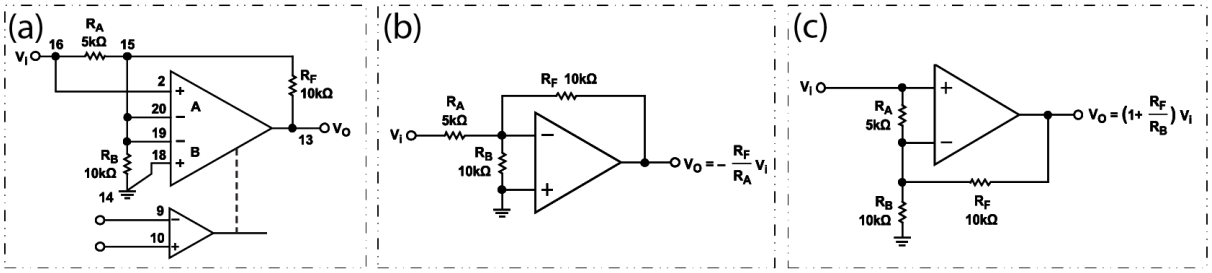

Figure 2: (a) AD630 symmetric gain (2). (b) Inverting gain configuration. (c) Non-inverting gain configuration.

In the present configuration, SEL B of voltage comparator is grounded and SEL A is connected to the reference signal followed by the phase shifter. When reference signal goes in its negative half cycle, Channel B is selected. This configuration acts as inverting amplification which yields gain of -2 whereas when reference signal goes in its positive half cycle, Channel A is selected. This is when the configuration achieves non–inverting amplification with a gain factor of $+2$.

1.4 Low Pass Filter

The demodulated signal generated by `AD630` passes through a `RC Low Pass Filter` which has a fixed RC resistance of 1 kΩ. The time constant τ can be changed to 1 s, 470 ms, 47 ms, 10 ms, 4.7 ms, 1 ms, 470 μs, 100 μs, 50 μs or 10 μs by changing a capacitor. The time constant of the low pass filter determines the bandwidth; larger the time constant, narrower is the bandwidth. This means that signals whose frequencies are within a tighter band around the reference signal will pass through, while others will be blocked.

2 Basic experimental tests of the Lock–In Amplifier

A sinusoidal waveform of amplitude 5 Vp of frequency 60 Hz is generated using a function generator and connected with a voltage divider circuit. This voltage divider circuit produces two frequency synchronized signals of amplitudes 5 Vp and 250 μVp. The 250 μVp signal is connected to the `BNC1` socket and the 5 Vp signal is connected to the `BNC2` socket of `PhysLock`. These signals are used as the input and reference signals for `PhysLock`. The whole configuration is shown in Figure 3.

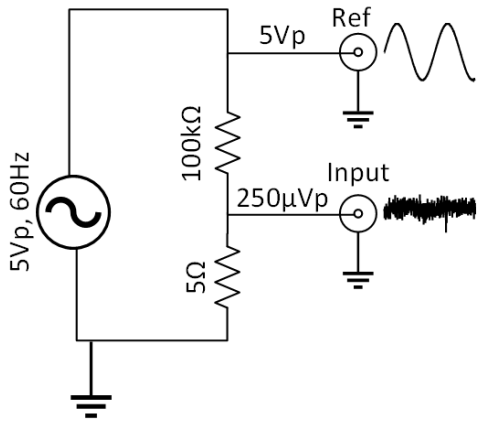

Figure 3: Configuration to produce two synchronized signals, one is used as the reference and other as input signal.

The 250 μVp signal produced in above configuration also includes noise in the millivolt regime. This signal is shown in Figure 4(a). The gain of input amplifier is set to 5000× which amplifies the reference input to 1.25 Vp (see Figure 4(b)). This amplified signal passes through the chip `AD630` followed by a low pass filter. Here switching between inverting and noninverting gain of the chip `AD630` is under the direct control of the reference signal. During the positive half cycle of the reference signal, `AD630` acts as a noninverting amplifier with a gain of 2, and during the negative half cycle, it acts as an inverting amplifier with a gain of −2. Figure 4(d) shows switching response of `AD630` on its pin 7 which is the output of the comparator controlling the inverting versus noninverting behavior of the input amplifier. Figure 4(e) shows the demodulated signal after passing through `AD630`, which appears as a positive rectified signal. The time constant of the low pass filter is set to 1 s with gain of 1, which converts this rectified AC signal to pure DC signal. This

DC signal is shown in Figure 4(f). We can switch between positive and negative rectified signals by changing the phase of the reference signal.

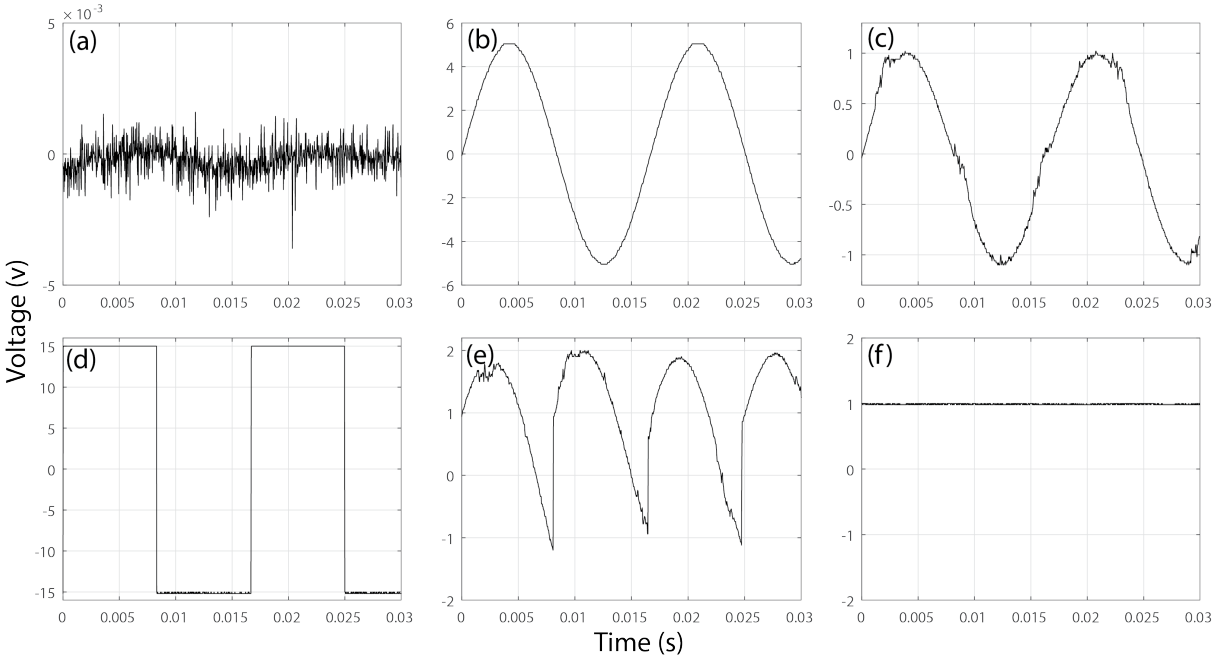

Figure 4: The test waveforms acquired different test points of `PhysLock`; (a) shows the input signal, (b) shows the reference signal, (c) shows the signal after passing through the input amplifier block, (d) shows `AD630`'s pin 07 (Test point) response which is the modulating waveform provided by the switching comparator, (e) shows demodulated signal after passing through `AD630`, and (f) shows the final output after passing through the low pass filter block.

3 Introduction to `PhysLock`'s Front Panel Controls

Typically, a lock-in amplifier measures the rms value of that component of input signal whose frequency is synchronized with the reference frequency. For example, suppose that the reference waveform is a sine wave of frequency 1 kHz. Furthermore the signal is a wave $A_1 \sin(2\pi \times 10^3 t) + A_2 \sin(2\pi \times 2 \times 10^3 t)$ + white noise. The output of an ideal lock–in should be a DC signal proportional to A_1, which is the component at the reference frequency. This should also be the case when the noise is much larger than A_1. Like any other lock–in, `PhysLock` also extracts and amplifies the DC signal but also provides output signals at several intermediate stages. This is how it gives the user more command over the instrument by displaying the performance of every stage of the process. Knobs and switches are provided to adjust different parameters of the process or to switch a part of the internal circuit on or off. BNC sockets are provided for displaying the signal on a voltmeter or an oscilloscope. We now describe the various front panel controls on `PhysLock`

3.1 End User Interface

See Figure 5 which shows different parts of the instrument. The purpose and usage of several important parts will now be described.

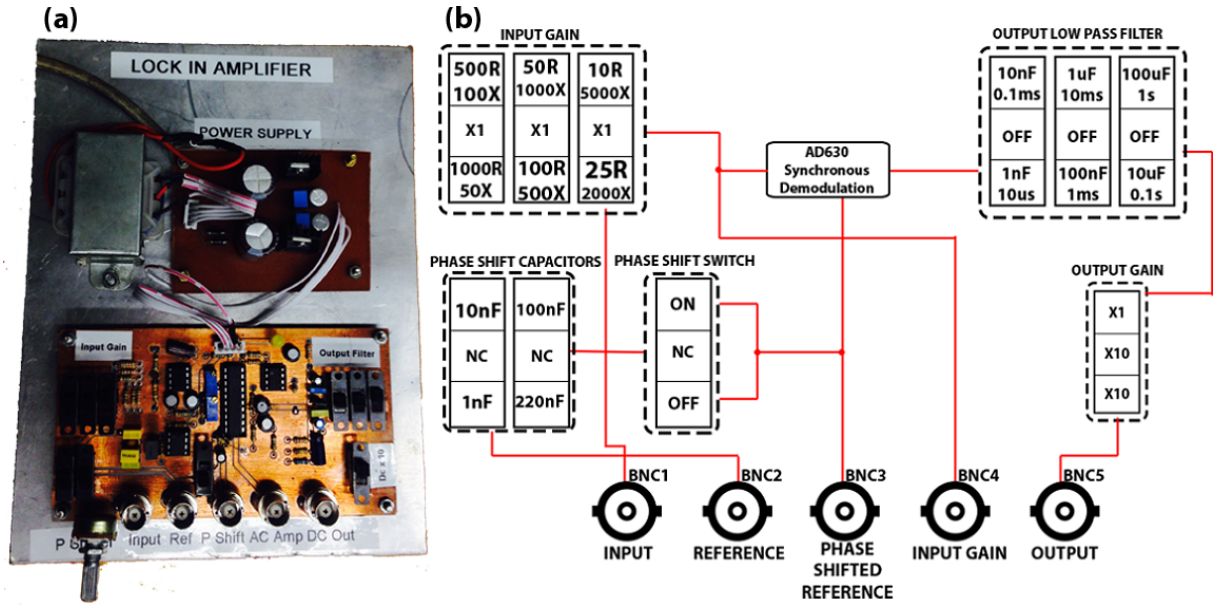

Figure 5: (a) Photograph of the instrument and (b) shows the schematic connections of the various input and output terminals with functional blocks of the instrument.

3.1.1 Phase Shift Switch

The phase shift in the reference signal can be turned on (Up) and off (Down) through the switch present in the "Phase Shift Switch" block. It is clear that turning the switch off will also disengage the phase shifter knob.

3.1.2 Phase Shift Adjustment

When the `Phase Shift Switch` is set on, the amount of the shift is given by

$$\phi = \pi - 2\tan^{-1}(\omega RC)$$

The provided dial adjusts R and the jumper switches present in the block "Phase Shift Capacitors" change the C capacitance. The phase shifted reference can be measured on the `BNC3` socket.

3.1.3 Input Gain

The AC input can be amplified to desirable level by using gain switches present in the "Input Gain" section and the amplified AC signal can be measured through the `BNC4 Connector`.

3.1.4 Output Low Pass Filter

These switches can be used to adjust the bandwidth (i.e. The 3 dB point) of the low pass filter applied to the output signal.

3.1.5 DC Gain

The DC gain switch amplifies the output signal by a factor of 10 (Down) or 1 (Up).

3.1.6 Reference

A square or sinusoidal wave of a known frequency is fed through this socket (labeled `BNC2`) which serves as the reference signal of the lock-in amplifier.

3.1.7 Input

The actual input signal to be analysed is connected on this socket which is labeled as `BNC1 Connector`.

3.1.8 DC Output

This is the ultimate output of the lock-in amplifier which has passed through all the stages with adjusted parameters. Normally, it should show a DC signal. However, if the signal shows some oscillating components, the low-pass filter should be adjusted.

4 Using `PhysLock` in an Optical Experiment: verifying Malus's law

To test our `PhysLock` in an optical setup, we used the configuration shown in Figure 5. An optical beam produced by a laser is passed through an optical chopper, which periodically interrupts the light beam with a frequency defined by the chopper's controller. This interrupted beam passes through the polarizer and the analyzer and is finally detected on a photodiode. The photodiode converts this interrupted optical signal into an electrical current which is converted to proportional voltage using a current-to-voltage amplifier.

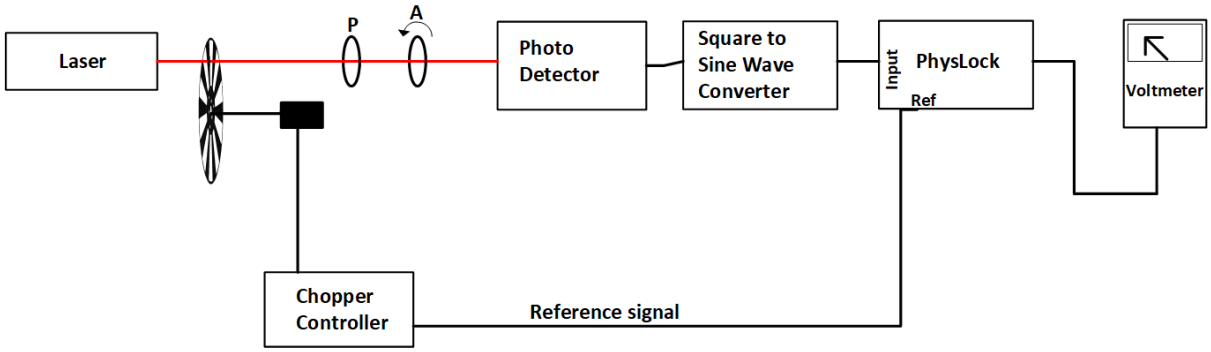

Figure 6: Schematic diagram of the experiment to verify the Malus's law where P represents the polarizer and A represents the analyzer.

The rectangular signal is converted into a sinusoidal signal by passing it through rectangular to sine wave converter. This ensures that the high frequency components (on the edges of square transitions) are removed. Remember that `PhysLock` shows optical performance at frequencies below 1 KHz. Finally, this signal along with a reference signal, taken from the chopper reference, is used to measure the DC value of that reference signal. Figure 7 shows the experimental curve which agrees almost perfectly with the theoretical prediction of the square of cosine relationship. In our experiment, we fixed the orientation of the polarizer while rotated the angle θ of the analyzer.

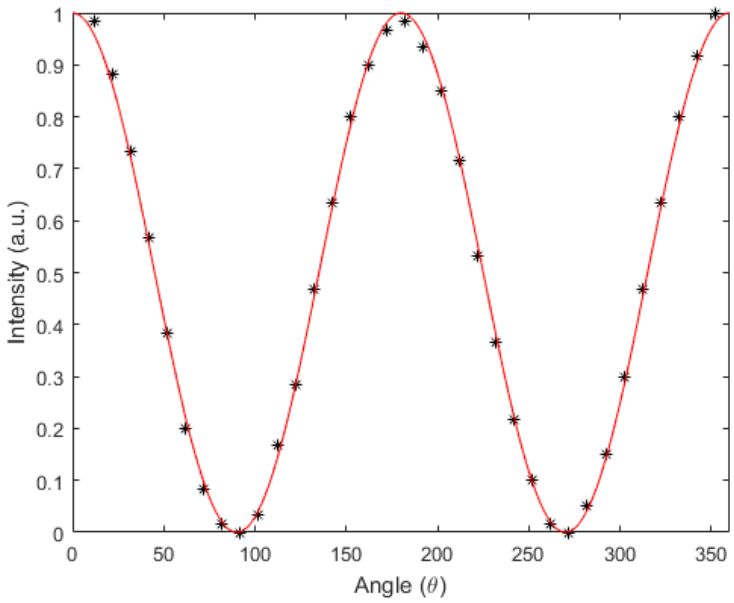

Figure 7: Intensity of an optical beam as a function of angle between two crossed polarizers, curve fitted on square of cosine, which satisfies Malus's law.

References

[1] https://www.analog.com/media/en/technical-documentation/data-sheets/ad630.pdf